RESEARCH DEPARTMENT

AN ELECTRONIC COUNTER SUITABLE FOR HIGH FREQUENCY OPERATION

Report No. T-056

(1955/16)

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SUMMARY

A binary counter has been developed which is characterised by a higher counting rate than that hitherto achieved. The report outlines the principles involved and describes a practical arrangement.

1. INTRODUCTION.

Some of the television systems[1] now under development include the use of a sub-carrier the frequency of which lies within the limits of the video spectrum.

The sub-carrier is in turn modulated by signals additional to and independent of those required by a normal black-and-white system and in order to reduce cross-talk between the modulated sub-carrier and the black-and-white signals to the minimum, the sub-carrier frequency is usually chosen to be an odd multiple of half the line-scanning frequency.

In such a television system, therefore, it is necessary to relate both line and field repetition frequencies to that of the sub-carrier. This may be effected by a chain of frequency dividers and multipliers, as illustrated in Fig. 1, where a sub-carrier, of frequency f_s, is generated in the unit A and is fed to a frequency-dividing and multiplying circuit B.

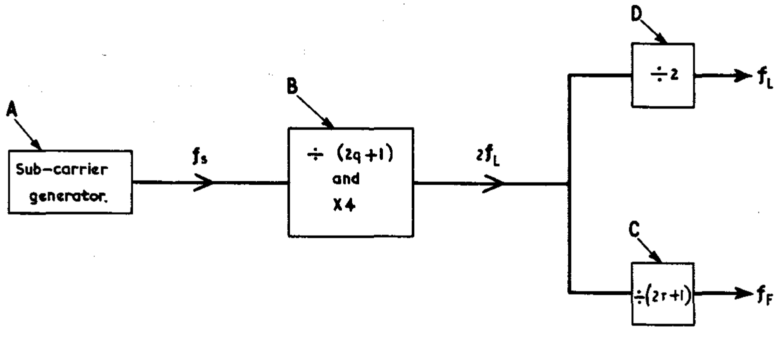

Fig. 1 - Arrangement of counters in a television system employing a band-shared sub-carrier

The frequency division effected in B has a divisor which is an odd integer, $(2q+1)$, and the divider output is, in the majority of systems[2], then multiplied by four. With suitable choice of f_s and q, the output from the multiplier can constitute a source of twice line-scan frequency $2f_L$ which may be fed to the customary field and line-frequency divider circuits (C and D). In the arrangement illustrated the field frequency f_F has been related to twice the line frequency by an odd integer $(2r+1)$, a condition necessary to produce the normal form of interlaced scanning raster.

The sub-carrier frequency chosen for a particular television system may (with British and American scanning standards) lie in the range 2-4 Mc/s, and it is necessary, therefore, that a frequency divider or counter should be developed which will accept an input within such a frequency range and operate satisfactorily when counting by a fairly large odd number which may be prime.

2. GENERAL CONSIDERATIONS.

A well known form of pulse counter or frequency divider which may be considered to fulfil the requirements listed above is the "triggered binary cascade"[3].

In such an arrangement each binary stage delivers one output pulse for every two input pulses. Evidently n such stages arranged in cascade will have an overall divisor or count of 2^n. If pulses derived from the output are re-inserted at suitable points, which may include the input, in such a manner that the added pulses occur during the intervals between the normal triggers, the cascade may be arranged to have an overall count equal to any integer between unity and 2^n. Such an arrangement is illustrated in Fig. 2, where the waveform diagrams show the derived feedback pulses added to the normal trigger pulses.

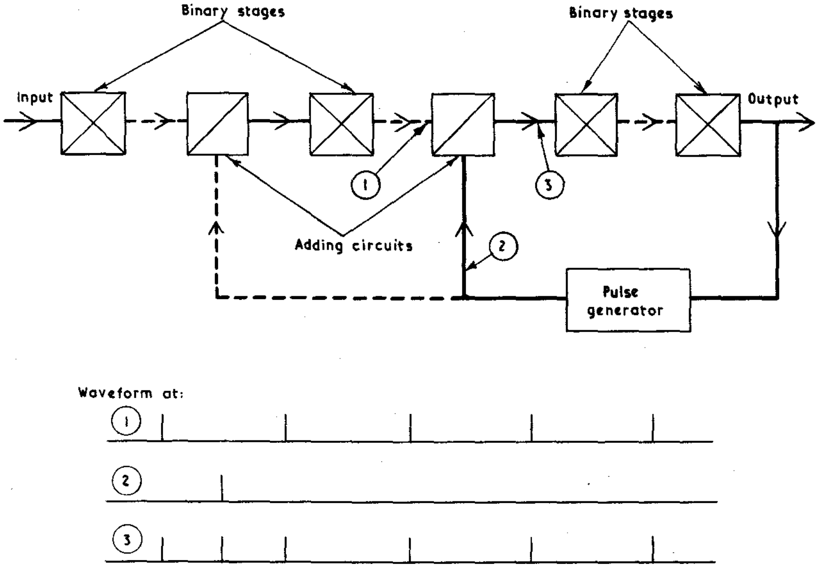

Fig. 2 - A binary cascade with additive feedback

The upper limit to the input pulse repetition frequency beyond which a binary cascade fails to operate satisfactorily is determined by two factors. First, due to the presence of stray reactance, triggering of the first binary stage will be followed by a finite recovery period during which the circuit will fail to respond to any further trigger. In these conditions, therefore, the maximum input repetition frequency will be such that the interval between input pulses just exceeds the duration of the first stage recovery period. Secondly, if feedback pulses derived from the cascade output are added to the input-pulse train, as shown in Fig. 2, the maximum usable input repetition frequency will fall to a value equal to or less than half that acceptable when operating without feedback. The factor of two relating these limits will result when the feedback pulse is arranged to occur exactly midway between two normal trigger pulses.

From the above discussion it will be seen that in order to satisfy the requirements demanded by the application described in Section 1 the first counter stage must be characterised by a recovery period equal to or less than 0·125 μ sec.

A modified form of the binary cascade counter[4] has been developed wherein the second of the two limiting factors described above has been eliminated.

3. THE GATED COUNTER.

In the modified arrangement a pulse, derived from the output of the cascade, is used to suppress one or more of the normal triggers driving various binary stages in the cascade. A simple example illustrating this principle is shown in Fig. 3, where a cascade of n stages is driven from the output of a gating circuit consisting of a simple electronic switch.

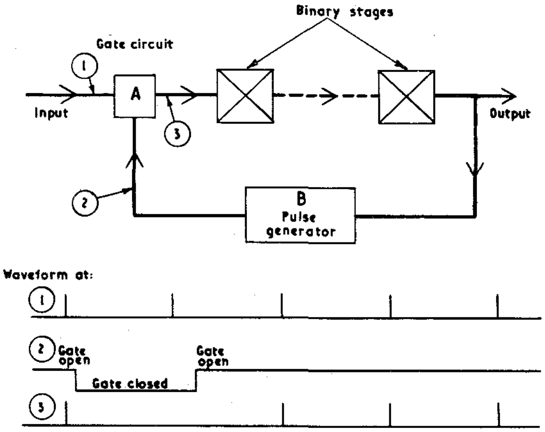

Fig. 3 - A binary cascade with gating feedback

Fig. 3 shows an input-pulse train (1) fed to a gate circuit A which is, in turn, operated by a control pulse (2) derived from the cascade output by means of the pulse generator B. The gate output waveform (3) constitutes the drive to a series of binary stages and if the cascade consists of n such stages, 2^n pulses of the waveform (3) will occur for every output pulse from the cascade. If each control pulse (2) is arranged to remove one pulse from the gate output, then each output pulse from the cascade will correspond to $2^n + 1$ pulses of the waveform (1). These operations are illustrated in the waveform diagrams of Fig. 3. It follows that if each control pulse is arranged to remove x input pulses, the overall count will be $2^n + x$. If the repetition frequency of the input pulses does not vary by more than one octave, the control pulse (2) may have a constant duration; however, operation may be made independent of input repetition frequency below a certain upper limit if the gate circuit A and the pulse generator B are of the form shown in Fig. 4.

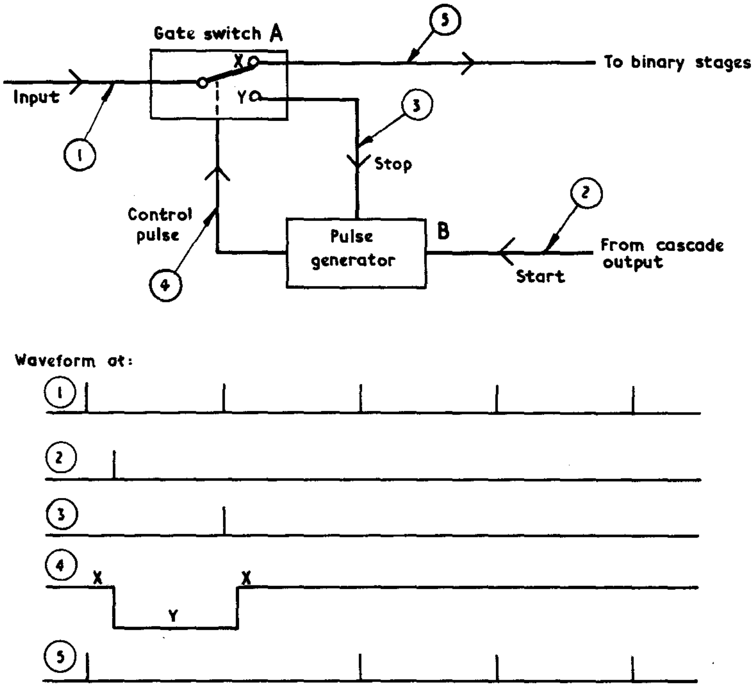

Fig. 4 - Automatic control of the gating pulse duration

In this case the gate circuit A is arranged as a double-throw electronic switch controlled, as before, from the pulse generator B. The switch normally connects the input waveform (1) to the binary cascade (switch position X). The cascade output pulse (2) is fed to the pulse generator B as a "start" pulse and initiates the control pulse (4) which, in turn, operates the electronic switch (position Y). The next input pulse is thus diverted into the pulse generator as a "stop" pulse (3). The waveform diagrams of Fig. 4 illustrate these operations and show that the trailing edge of the control waveform always occurs immediately following the trailing edge of the pulse gated out. A pulse counter may be inserted in the "stop" pulse circuit, in order that the gate circuit may remove two or more pulses per operation.

In a general arrangement several such gate circuits may be inserted at various points in the binary cascade. Each of these gate circuits may then be operated by suitable control pulses derived from the cascade output.

In can be shown (see Appendix) that if such an arrangement contains n binary stages, where each stage is preceded by a gate circuit removing one input pulse per cascade output pulse, the count may be arranged to have any integral value between 2^n and $2^{n+1}-1$.

4. A PRACTICAL EXAMPLE.

A complete counter, based upon the principles outlined, has been developed in connection with an investigation into the properties of "dot-interlace"[5] as a bandwidth-saving device. Such an application is very similar in requirements to those outlined in Section 1 although, in this case, the operating range of input-pulse repetition frequency is somewhat higher. A block schematic diagram of the counter (Fig. 5) shows a cascade of four binary stages arranged to count by any integer within the limits of 16 and 31 inclusive.

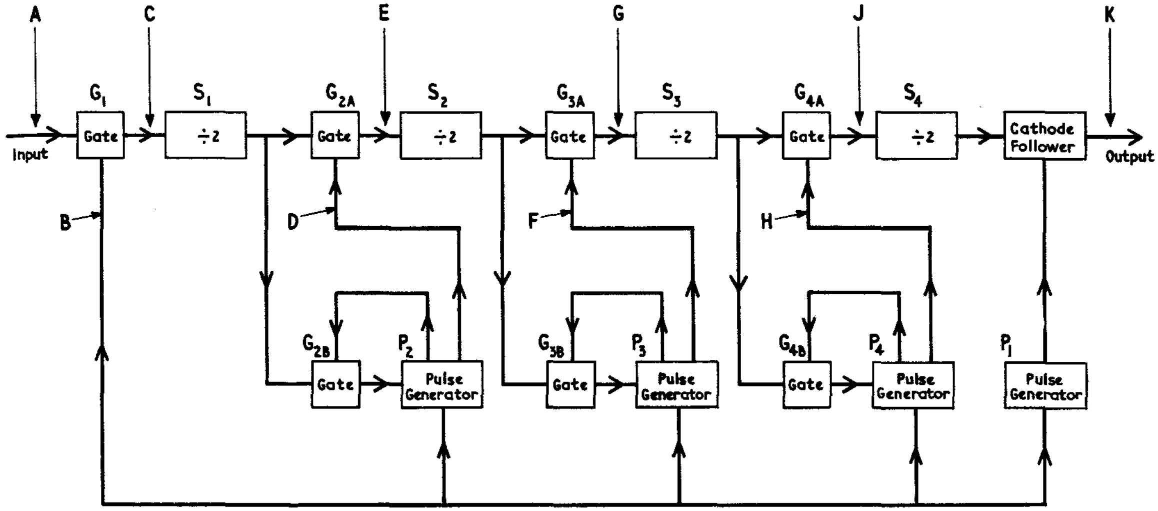

Fig. 5 - A schematic diagram of a gated counter

The input-pulse train is applied to the first gate circuit G1 wherein one input pulse may be removed for each gating pulse derived from P1, that is, for each cascade output pulse. The output of the gate G1 drives the first binary stage S1.

Short pulses representing the output of S1 now form the input to the double-throw switch circuit formed by G2A and G2B. The principle of operation of this arrangement has been outlined above and illustrated in Fig. 4. The two gates G2A and G2B have identical input waveforms but are operated by control pulses of opposite polarity such that in the normal condition G2A is open and G2B is closed. A cascade output pulse fed through P1 will actuate P2 causing G2A to close and G2B to open. The next input pulse to the gates will now be routed to P2 thus terminating the control pulse. The circuit has now been returned to the normal condition (G2A open, G2B closed) and will remain so until the next cascade output pulse.

The remaining binary and gate stages of the cascade are similar in design and performance. By means of switches each of the gating circuits may be arranged either to remain open continuously or to operate as described. Thus one stage input pulse per cascade output pulse may be removed at will from the input to any of the binary stages in the cascade. In this way the cascade count may be varied over the range of 16 (all gates open continuously) to 31 (all gates pulse-operated) inclusive.

In order to furnish more detailed design information, circuits of the basic binary stage and the two forms of gating arrangement are described below.

4.1. The Binary Stage.

Fig. 6 shows the circuit of a binary stage as incorporated in the cascade. The valves V1, V2 and V3 form a directly coupled multivibrator wherein the cross

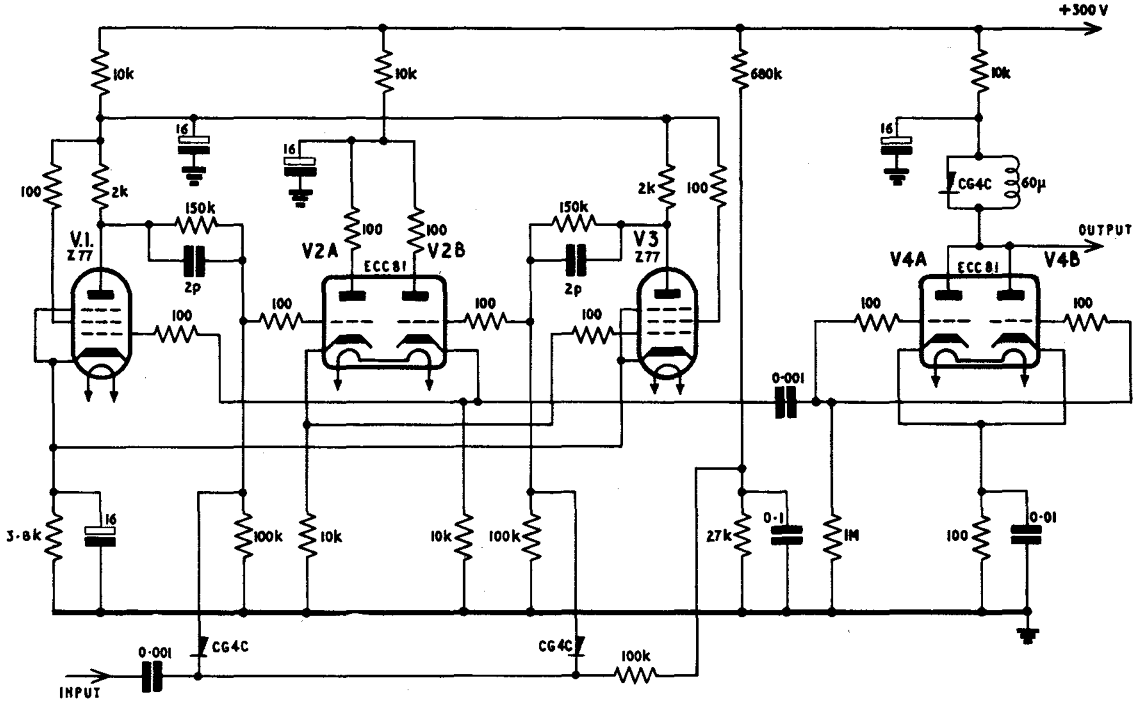

Fig. 6 - A binary stage suitable for high frequency operation

coupling feedback paths are routed through the cathode followers formed by V2A and V2B. By this means the recovery time of the circuit is reduced to a minimum in that grid current in either V2 or V3 cannot cause charging of the cross coupling condensers. In addition, the capacitance appearing across the load resistors of V1 and V3 is reduced to a minimum. The input pulses, of negative polarity, are applied through crystal rectifiers to the grids of the cathode followers V2A and V2B. The bias on the rectifiers is such that a negative input pulse is applied to that grid of V2 having the greater positive potential with respect to earth. The rectangular voltage waveform appearing at the cathode of V2B forms the drive to V4. The resulting anode current of V4 flows through the pulse-generating circuit formed by the resonance of the anode load inductance with stray capacitance. A crystal rectifier is connected in such a way as to damp all oscillation other than that resulting from a cessation of anode current in V4. A positive voltage pulse of half-sinusoid shape appears at the anode of V4 for every two pulses applied at the stage input.

4.2. The Gating Circuits.

As will be evident from Fig. 5, two types of gating arrangement are utilised in the complete counter. The first, used in the gate G1, is of the type discussed with reference to Fig. 3 and consists simply of an amplifier accepting input trigger pulses of positive sign at the control grid and control pulses of negative polarity at the suppressor grid. A control switch is provided whereby the control pulses may be removed from the suppressor grid, resulting in a continuous and uninterrupted pulse output from the gate. Control pulses of positive polarity are derived from the pulse generator P1 (Fig. 5) wherein the rectangular waveform at the cascade output is converted into a train of pulses having a duration, polarity and timing such that the gate G1 removes one cascade input pulse for each cascade output pulse. The circuit arrangement used for P1 is very similar to that associated with V4 in Fig. 6. The output pulses from P1 are also used as trigger pulses for the other gates (G2, G3 and G4) in the counter. The circuit arrangement used for these gates is of the type illustrated in Fig. 4 and a detailed circuit diagram of one such stage is shown in Fig. 7.

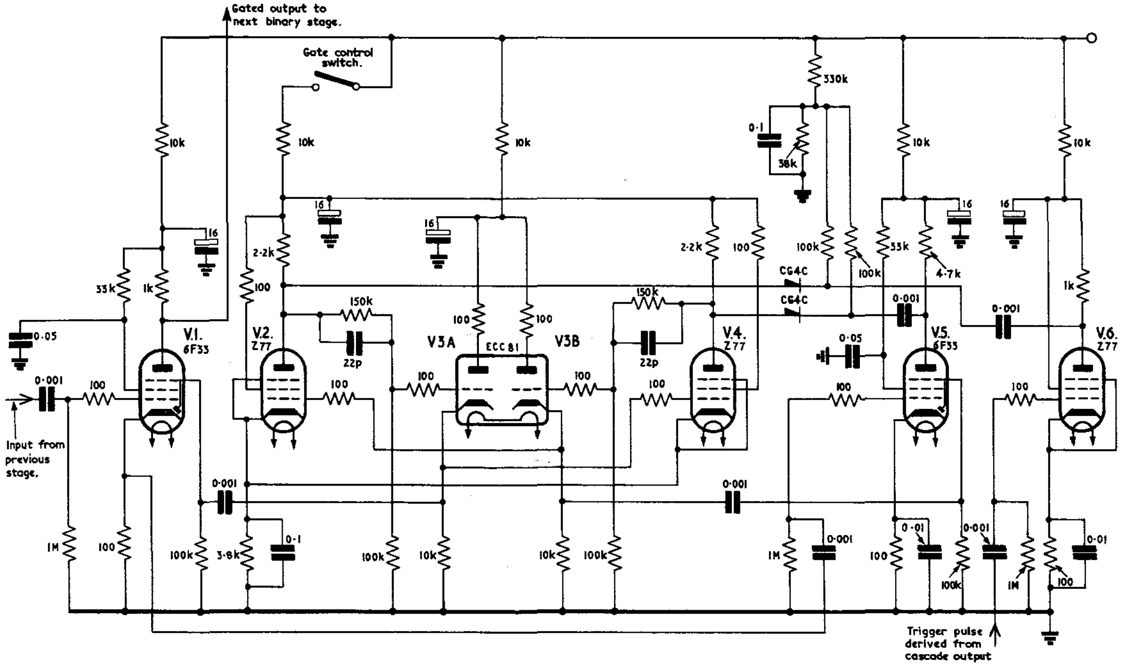

Fig. 7 - A high speed single-pole two-way gating circuit

Input pulses of positive polarity are applied to the control grid of V1 and, in the absence of gating pulses at the suppressor grid, are passed from the anode circuit of V1 to the next binary stage (Fig. 4, gate switch A, position X). The ungated input pulses appear at the cathode of V1 and are fed to an amplifier V5. At this point in the discussion it will be assumed, for the sake of simplicity, that the high-speed bi-stable stage formed by V2, V3 and V4, is in that state of equilibrium where V2 is cut off and V4 conducting. A trigger pulse derived from the cascade output is amplified in V6 and is passed through a suitably biased crystal rectifier to the anode of V2, causing a change in the circuit conditions of V2, V3 and V4 such that V2 conducts and V4 is cut off. The resulting negative-going voltage transition occurring at the cathode of V3A is fed to the suppressor grid of V1, cutting off the pulse drive to the following binary stage. A similar transition of positive polarity appearing at the cathode of V3B is fed to the suppressor grid of V5 such that the next input pulse appears at the anode of V5 (Fig. 4, gate switch A, position Y). This pulse, fed through a suitably-biased rectifier, causes the bi-stable circuit to revert to the first condition of equilibrium. The resulting positive-going voltage transition at the cathode of V3A terminates the gating pulse to V1 and a similar negative transition at the cathode of V3B results in anode current cut-off in V5.

The circuit has thus completed one gating cycle and will repeat the above operations whenever a trigger pulse is received from the cascade output. It will be appreciated that the circuit shown relies on rectification for bias setting at the grids of the coincidence gates V1 and V5. The rectification is effected either by grid current or by means of anode current in auxiliary diodes. The grid time-constants shown are suitable for operation with a cascade whose output repetition frequency is fairly high and these constants should be increased when the gating circuit is required to operate at lower repetition frequencies.

As in the case of the gate G1, all the remaining gate circuits are provided with a control switch whereby the gating process may be discontinued. Such a switch is shown in Fig. 7, in series with the H.T. supply to valves V2 and V4. When this switch is opened gating pulses are removed from the suppressor grid of V1.

5. RESULTS AND CONCLUSIONS.

The complete counter unit, as outlined above and illustrated schematically in Fig. 5, has proved to be fully practicable and reliable. In order to provide some evidence of correct operation and to illustrate further the operating sequence, a series of oscilloscope photographs is provided in Fig. 8. The traces show waveforms at various points in the complete circuit when an input-pulse train having a repetition frequency of 5·5 Mc/s is applied to the counter, a value of input repetition frequency equal to the video sampling rate used in some experiments carried out on a "dot interlace" television system as mentioned in Section 4.

In the waveforms illustrated all the gate circuits are in the pulse-operated condition and as there are four binary stages ($n = 4$) the overall divisor has the value 31 ($2^{n+1}-1$). Thus for an input repetition frequency of 5·5 Mc/s the repetition frequency at the output will be 177 kc/s.

The code letters beside each photograph refer to a similar set in Fig. 5 and illustrate the waveforms appearing at the corresponding points indicated in that schematic diagram.

A counting arrangement of the type described should prove valuable in many applications, particularly where high operating frequencies are encountered. The circuit provides convenient means for changing the overall count, a feature which may prove valuable in future colour television systems. Further developments of the arrangement can effect a saving in the total number of valves employed.

A complete counter based on the foregoing work has been built and has given trouble free operation since its inception, a period of 700 working hours.

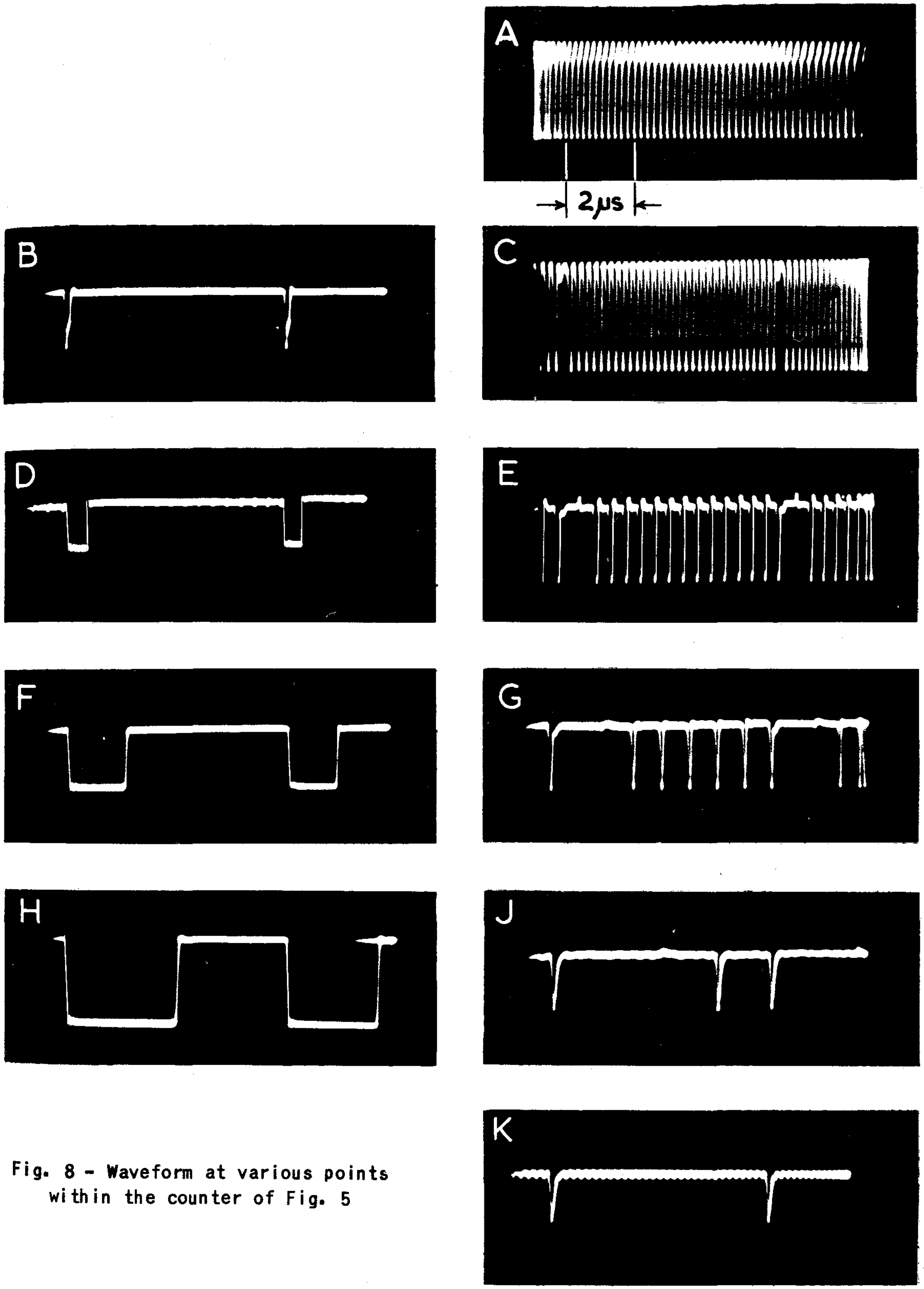

Fig. 8 - Waveform at various points within the counter of Fig. 5

6. REFERENCES.

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2. Abrahams, I.C., "Choice of Chrominance Sub-carrier Frequency in the N.T.S.C. Standards", Proc. I.R.E., Vol. 42, No. 1, January 1954.

3. Lord, A.V. and Wood, C.B.B., "A Variable Definition Camera Channel for the Appraisal of Television Standards", Proc. I.E.E., Part IIIA, No. 20, p. 811, April-May 1952.

   Research Department Report No. T-025, 1949.

4. Patent Application 17897/52.

5. Wilson Boothroyd, "Dot Systems of Colour Television", Electronics, Part I, p. 88, December 1949.

   Haantjes, J. and Teer, K., "Multiplex Television Transmission", Wireless Engineer, Parts I and II, September and October 1954.

APPENDIX

Fig. 9 shows an arrangement of n binary stages, a gating circuit being provided at the input of certain stages.

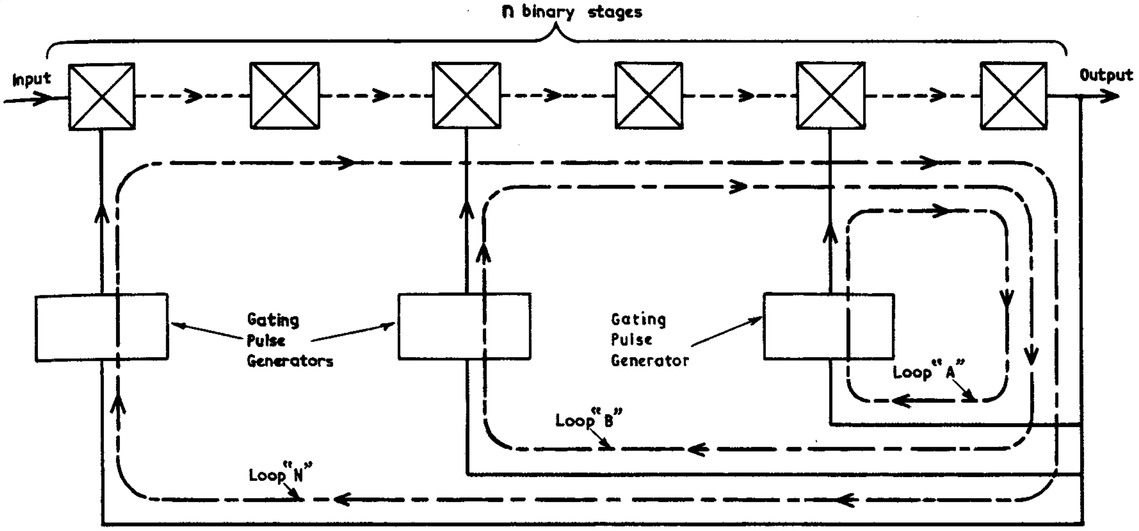

Fig. 9 - A general arrangement of gating binary stages in a gated counter

For the purpose of analysis, loops A, B and N are indicated in the diagram, loop A embracing a stages, loop B embracing b stages, etc.

If each cascade output pulse suppresses one input pulse at the first gate in each loop, the divisor D_A of loop A will be

$$D_A = 2^a + 1 \tag{1}$$

For loop B

$$\begin{aligned} D_B &= 2^{b-a}\ (2^a + 1) + 1 \\ &= 2^b + 2^{b-a} + 1 \end{aligned}$$

Similarly for loop N

$$D_N = 2^n + 2^{n-a} + 2^{n-b} + 2^{n-c} + \ldots\ldots + 2^{n-m} + 1$$

where m is the number of binary stages enclosed by the penultimate loop. In general

$$D_N = 1 + 2^n + \sum_{\lambda=m}^{a} 2^{n-\lambda} \tag{2}$$

When all stages of the cascade are each preceded by a gating circuit removing one stage-input pulse per cascade-output pulse, the total number of loops will equal the total number of stages n.

continued overleaf